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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,622	07/26/2004	Tai-Yuan Chen	12475-US-PA	4621

31561 7590 10/10/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
STEVENSON, ANDRE C	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,622	CHEN, TAI-YUAN	
	Examiner	Art Unit	
	Andre' C. Stevenson	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22-31* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/26/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims #1-19 and 22-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsumoto et al. (U.S. Pub. No.2004/0058540 A1, Pub. Date 03/25/04, Filed 09/18/03).

Matsumoto substantially shows the claimed invention, as shown in figures #1-23 and corresponding text, **pertaining to claim #1**, a method of correcting a lithographic process, comprising the steps of performing a physical vapor deposition (PVD) process to form a thin film over a wafer **(Page #8, paragraph 0138; Page #10, paragraph 0144)**, wherein an overlay mark on the wafer has a positional shift that depends on the target consumption in the PVD process and a formula relating the two can be derived **(Page #5, paragraph 0079; Page #10, paragraph 0144)**; obtaining a compensation value from the formula **(Page #1, paragraph 0013)**; forming a photoresist layer **(item #202)** over the thin film **(item #203)**; and performing a lithographic process to pattern the photoresist layer **(Page #8, paragraph 0139; Page #9,**

paragraph 0141), wherein the compensation value is fed back to correct parameters used in lithographic process **(Page #1, paragraph 0013; Page #6, paragraph 0106; Page #5, paragraph 0079; Page #8, paragraph 0136).** ***Pertaining to claim #2,*** Matsumoto shows a method wherein the step of obtaining the compensation value comprises obtaining a compensation value for each wafer **(Page #10, paragraph 0144).** ***Pertaining to claim #3,*** Matsumoto shows a method wherein the step of obtaining the compensation value comprises obtaining a compensation value for each batch containing a specific number of wafers **(Page #10, paragraph 0144).** The Examiner notes that Matsumoto fails to mention explicitly, obtaining a compensation value for each batch containing a specific number of wafers. However, Matsumoto shows a method for obtaining a compensational value for each wafer. The Examiner takes the position that the because the method of Matsumoto performs this task for each wafer and compiles the information, that Matsumoto indeed does collect and calculate the value for the entire batch. For these reasons, the Examiner takes the position that the rejection is proper. ***Pertaining to claim #4,*** Matsumoto shows, a method further comprising determining a constraint on the operating recipe parameter and wherein minimizing the objective, function further comprises minimizing the objective function subject to the constraint on the operating recipe parameter **(Page #4, paragraph 0072; Page #2, paragraph 0026).** ***Pertaining to claim #5,*** Matsumoto shows a method wherein the control system further records the target consumption in each PVD process and corresponding shift in overlay mark position so that the formula can be renewed **(Page #10, paragraph 0147).** ***Pertaining to claim #6,*** Matsumoto shows a method wherein the control system comprises an advanced process control (APC) system **(Figure #19; Page #9, paragraph 0141; Page #2, paragraph 0026; Page #4, paragraph 0072).** ***Pertaining***

to claim #7, Matsumoto shows a method wherein the positional shift is in a direction towards a center of the wafer **(Page #4, paragraph 0075; Page #1, paragraph 0013).** The Examiner notes that Matsumoto does not mention explicitly that the positional shift is in a direction towards the center of the wafer. However, Matsumoto shows a method wherein the difference is calculated using the differentials dy and dx, which are bi-directional and can be in the positive or negative direction. The Examiner takes the position that Matsumoto shows finding the difference in positional shift in either the Y or X direction, both directed towards the center and away from it. For this reason, the Examiner takes the position that the rejection is proper. ***Pertaining to claim #8,*** Matsumoto shows a method wherein the positional shift is in a direction away from a center of the wafer **(Page #8, paragraph 0130).** ***Pertaining to claim #9,*** Matsumoto shows a method wherein the positional shift is a rotational shift **(Page #5, paragraph 0090, Page #11, Claim #7; Page #5).** ***Pertaining to claim #10,*** Matsumoto shows, a method of forming an overlay mark on a wafer having a material layer thereon, comprising the steps of: forming a opening pattern in the material layer to serve as an outer mark; forming a first film layer on the material layer; removing a portion of the first film layer to expose a portion of the material layer; performing a physical vapor deposition (PVD) process to form a second film layer over the first film layer, wherein the deposited second film layer causes a shift in an over-lay mark such that the degree of shifting is related to the target consumption in the PVD process and a formula relating the two can be derived; obtaining a compensation value from the formula; forming a photoresist layer over the second film layer; and performing a lithographic process to form an inner mark, wherein the compensation value is fed back to correct parameters used in lithographic process **(Page #8, paragraph 0138; Page #10, paragraph 0144; Page #5, paragraph 0079; Page #1, paragraph**

0013; Page #8, paragraph 0139; Page #9, paragraph 0141; Page #1, paragraph 0013; Page #6, paragraph 0106; Page #5, paragraph 0079; Page #8, paragraph 0136). ***Pertaining to claim #11,*** Matsumoto shows a method wherein the step of obtaining the compensation value comprises obtaining a compensation value for each wafer **(Page #10, paragraph 0144).** ***Pertaining to claim #12,*** Matsumoto shows a method wherein the step of obtaining the compensation value comprises obtaining a compensation value for each batch containing a specific number of wafers **(Page #10, paragraph 0144).** The Examiner notes that Matsumoto fails to mention explicitly, obtaining a compensation value for each batch containing a specific number of wafers. However, Matsumoto shows a method for obtaining a compensational value for each wafer. The Examiner takes the position that the because the method of Matsumoto performs this task for each wafer and compiles the information, that Matsumoto indeed does collect and calculate the value for the entire batch. For these reasons, the Examiner takes the position that the rejection is proper. ***Pertaining to claim #13,*** Matsumoto shows a method wherein the formula relating the target consumption and degree of shifting is recorded within a control system that also computes the compensation value and feeds the compensation value back to correct the lithographic operation **(Page #4, paragraph 0072; Page #2, paragraph 0026).** ***Pertaining to claim #14,*** Matsumoto shows a method wherein the control system further records the target consumption in each PVD process and corresponding shift in overlay mark position so that the formula can be renewed **(Page #10, paragraph 0147).** ***Pertaining to claim #15,*** Matsumoto shows a method wherein the control system comprises an advanced process control (APC) system **(Figure #19; Page #9, paragraph 0141; Page #2, paragraph 0026; Page #4, paragraph 0072).** ***Pertaining to claim #16,*** Matsumoto shows a method wherein the shift is

in a direction towards a center of the wafer **(Page #4, paragraph 0075; Page #1, paragraph 0013).** The Examiner notes that Matsumoto does not mention explicitly that the positional shift is in a direction towards the center of the wafer. However, Matsumoto shows a method wherein the difference is calculated using the differentials dy and dx, which are bi-directional and can be in the positive or negative direction. The Examiner takes the position that Matsumoto shows finding the difference in positional shift in either the Y or X direction, both directed towards the center and away from it. For this reason, the Examiner takes the position that the rejection is proper. ***Pertaining to claim #17,*** Matsumoto shows a method wherein the shift is in a direction away from a center of the wafer **(Page #8, paragraph 0130).** ***Pertaining to claim #18,*** Matsumoto shows a method wherein the shift is a rotational shift **(Page #5, paragraph 0090, Page #11, Claim #7; Page #5).** ***Pertaining to claim #19,*** Matsumoto shows a method wherein the material layer comprises an insulation material layer **(Page #10, paragraph 0144).**

Pertaining to claim #20, Matsumoto shows a method wherein comprises a first metallic layer the first film layer **(Page #8, paragraph 0138).** ***Pertaining to claim #22,*** Matsumoto shows, a method of correcting a lithographic process, comprising the steps of: performing a physical vapor deposition (PVD) process to form a thin film over a wafer, wherein an overlay mark on the wafer has a positional shift that depends on the target consumption in the PVD process and a formula relating the two can be derived; obtaining a compensation value from the formula; forming a photoresist layer over the thin film; combining the first compensation value with the data in a lithographic correction system to produce a second compensation value; and performing a lithographic process to pattern the photoresist layer, wherein the second compensation value is fed back to correct parameters used in lithographic process **(Page #8,**

paragraph 0138; Page #10, paragraph 0144; Page #5, paragraph 0079; Page #1, paragraph 0013; Page #8, paragraph 0139; Page #9, paragraph 0141; Page #1, paragraph 0013; Page #6, paragraph 0106; Page #5, paragraph 0079; Page #8, paragraph 0136). ***Pertaining to claim #23,*** Matsumoto shows a method wherein the step of obtaining the first compensation value comprises obtaining a first compensation value for each wafer **(Page #10, paragraph 0144).** ***Pertaining to claim #24,*** Matsumoto shows a method wherein the step of obtaining the first compensation value comprises obtaining a first compensation value for each batch containing a specific number of wafers **(Page #10, paragraph 0144).** The Examiner notes that Matsumoto fails to mention explicitly, obtaining a compensation value for each batch containing a specific number of wafers. However, Matsumoto shows a method for obtaining a compensational value for each wafer. The Examiner takes the position that the because the method of Matsumoto performs this task for each wafer and compiles the information, that Matsumoto indeed does collect and calculate the value for the entire batch. For these reasons, the Examiner takes the position that the rejection is proper. ***Pertaining to claim #25,*** Matsumoto shows, a method wherein the formula relating the target consumption and degree of shifting is recorded within a control system that also computes the first compensation value and feeds the second compensation value back to correct the lithographic operation **(Page #4, paragraph 0072; Page #2, paragraph 0026).** ***Pertaining to claim #26,*** Matsumoto shows a method wherein the control system further records the target consumption in each PVD process and corresponding shift in overlay mark position so that the formula can be renewed **(Page #10, paragraph 0147).** ***Pertaining to claim #27,*** Matsumoto shows a method wherein the control system comprises an advanced process control (APC) system **(Figure #19; Page #9, paragraph**

0141; Page #2, paragraph 0026; Page #4, paragraph 0072). ***Pertaining to claim #28,*** Matsumoto shows a method wherein the positional shift is in a direction towards a center of the wafer **(Page #4, paragraph 0075; Page #1, paragraph 0013).** The Examiner notes that Matsumoto does not mention explicitly that the positional shift is in a direction towards the center of the wafer. However, Matsumoto shows a method wherein the difference is calculated using the differentials dy and dx, which are bi-directional and can be in the positive or negative direction. The Examiner takes the position that Matsumoto shows finding the difference in positional shift in either the Y or X direction, both directed towards the center and away from it. For this reason, the Examiner takes the position that the rejection is proper. ***Pertaining to claim #29,*** Matsumoto shows a method wherein the positional shift is in a direction away from a center of the wafer **(Page #8, paragraph 0130).** ***Pertaining to claim #30,*** Matsumoto shows a method wherein the positional shift is a rotational shift **(Page #5, paragraph 0090, Page #11, Claim #7; Page #5).** ***Pertaining to claim #31,*** Matsumoto shows a method wherein the data in the lithographic correction system comprises the data obtained from a photo-exposure station **(Page #4, paragraph 0070).**

Allowable Subject Matter

Claim #21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, **depending on further search.**

Claim #21 **depending upon further search.**

- ✓ A method wherein employing the control equation further comprises employing a non-linear control equation.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure; MeDevitt et al. (U.S. Pub. No. 2003/0064422), Clark (U.S. Pub. No. 2004/0197939).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

(703) 872-9306

Andre' Stevenson

09/28/06

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER